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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,903	03/01/2005	Martin Vorbach	2885/87	6927

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EXAMINER	
WANG, JUE S	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
05/25/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/501,903	VORBACH ET AL.	
	Examiner	Art Unit	
	JUE WANG	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/24/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 have been examined.

Information Disclosure Statement

2. The information disclosure statement filed 2/24/2010 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. Specifically, a copy was not provided for the non-patent literature publications Becker, J., "Configurable System-on-Chip (CSoC)" (item 6 on page 3) and Cook, Jeffery J., "The Amalgam Compiler Infrastructure" (item 12 on page 3). Accordingly, these two non-patent literature publications have not been considered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker et al. "Automatic Parallelism Exploitation for FPL-based Accelerators" (hereinafter Becker), in view

of Hartenstein et al. "A Two-level Co-Design Framework for Xputer-based Data-driven Reconfigurable Accelerators" (hereinafter Hartenstein).

5. As per claim 1, Becker teaches the invention as claimed, including a method for partitioning large computer programs and or algorithms at least part of which is to be executed by an array of reconfigurable units including a plurality of Arithmetic Logic Units (ALUS) (see page 170. Figure 2, right column, paragraphs 2, 3, page 171, Figure 4), comprising the steps of

defining a maximum allowable size to be mapped onto the array (see page 176, left column, paragraph 2; EN: the vectorization factor is the maximum allowable size),

partitioning the program such that its separate parts minimize the overall execution time and providing a mapping onto the array not exceeding the maximum allowable size (see page 172, right column, paragraph 1, pages 173, left column, paragraph 3, page 174, right column, last paragraph, page 176, left column, paragraphs 2-4; EN: the program is partitioned into a sequence of maximal parallelized execution units according to the granularity of the architecture and the hardware constraints and using a scheduling algorithm to minimize total execution time under resource constraints).

Becker does not explicitly state that the array of reconfigurable units include a plurality of memory units. However, it is obvious that the xputer target platform of Becker would contain a plurality of memory units as it is well known in the art that the xputer target platform contains a plurality of memory units (i.e., ALU array including several rALU subnets for multiple scan windows where the scan windows are memory units, see page 4, left column, paragraphs 2 and 4 of Hartenstein).

6. As per claims 2 and 3, the limitations recited in these claims are substantially similar to those recited in claim 1. Therefore, they are rejected using the same reasons as claim 1.

7. As per claim 4, Becker teaches the reconfigurable processing units are arithmetic logic units (see page 170, Figure 2, right column, paragraph 2).

Response to Arguments

8. Rejection of claims under §103(a):

9. As per independent claims 1-3, Applicants arguments have been fully considered but are moot in light of the new grounds of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Hartenstein et al. "Parallelizing Compilation for a Novel Data-Parallel Architecture", 1995, PCAT-94, Parallel Computing: Technology and Practice.
- Jurgen Becker, "A Partitioning Compiler for Computers with Xputer-based Accelerators", 1997, Kaiserslautern University.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jue S. Wang whose telephone number is (571) 270-1655. The examiner can normally be reached on M-Th 7:30 am - 5:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lewis A. Bullock, Jr./
Supervisory Patent Examiner, Art Unit 2193

Jue Wang
Examiner
Art Unit 2193